

How Quickly Will Multi-Die Systems Change Semiconductor Design?

The view of keystone companies driving the future of multi-die systems

EXECUTIVE SUMMARY

For many decades, semiconductor design and implementation has been focused on monolithic, ever-larger and more complex single-chip implementation. This system-on-chip approach is now changing for a variety of reasons. The new frontier utilizes many chips assembled in new ways to deliver the required form-factor and performance.

Multi-die systems are paving the way for new types of semiconductor devices that fuel new products and new user experiences.

This Synopsys Industry Insight brings together a select group of keystone companies who are advancing multi-die systems. You'll read the thoughts of senior executives from various levels of the technology stack. You'll also hear from Synopsys' CEO, its president and a panel of Synopsys technology experts. We'll discuss our achievements, what lies ahead and how we are partnering with the industry to drive change.

Read on to discover how multi-die systems are evolving and being adopted by the semiconductor industry. This technology is likely to become ubiquitous in the very near future to enable every product you own, and some new ones you will want to own.

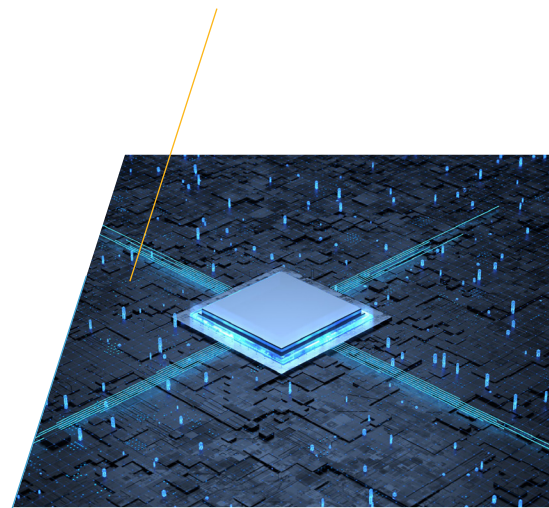


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CHAPTER 1

SYSMOORE: SYSTEMIC COMPLEXITY WITH A MOORE'S LAW AMBITION!

The semiconductor industry has driven the single biggest rate of change in the history of mankind. Gordon Moore, with his prediction turned to 'law,' captured the very *Gestalt* of our industry as 'exponential scale ambition.' He thus became not only a visionary, but also our coach by implicitly expecting us to **'build the impossible'** – and we did!

At Synopsys, we have fueled this exponential ambition by enabling over 10,000,000x productivity in chip design. The transition from 'Computer Aided Design' to 'Electronic Design Automation' is overlaid in figure 1. The last decade has rapidly adopted machine learning everywhere and powerful AI has now automated entire sub-flow design!

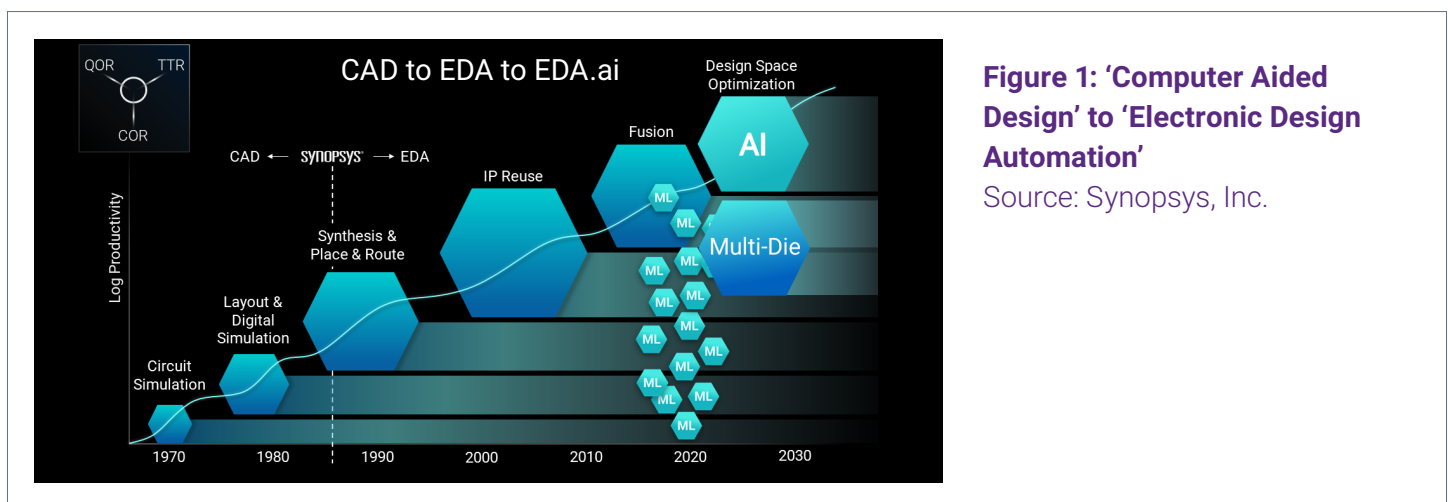
While, in recent years, the exponential growth has slowed substantially, the demand for more computation has not. On the contrary! The exploding impact of 'Smart Everything' powers a massive push for continued speed and transistor count increases.

To make technology supply meet economic demand, system architects are revolutionizing both architectural function and form. To drive speed and efficiency, 'function' is now completely defined by the target software. Even in automotive, the term 'software defined cars' is commonplace! Louis Sullivan, an architect from the late 1800's, stated, "form follows function." And indeed, in semiconductors, the single-chip 'form' now shifts to **multi-die**, thus unleashing the **SysMoore** era: Systemic Complexity with a Moore's Law ambition!



Aart de Geus

Chair and Chief Executive Officer,
Synopsys



Interestingly, Sullivan's draftsman, the later well-renowned architect, Frank Lloyd Wright stated that "form and function should be one." We resonate strongly with this perspective as the complex selection of which functionality to put in with each die, technology, and connectivity mechanisms are the very choices that define systemic complexity and will lead to enormous future capabilities!

This all begs the question, "why now?" Through a technomic lens, we continue to align technology breakthroughs and economic opportunities. While in Classic Moore's Law, transistor sizes shrunk over decades, the recent multi-die connectivity advances are just as astounding. Take note that the connectivity density featured in figure 2 increase, while the switching energy per bit decrease, this can only be viewed as fantastic.

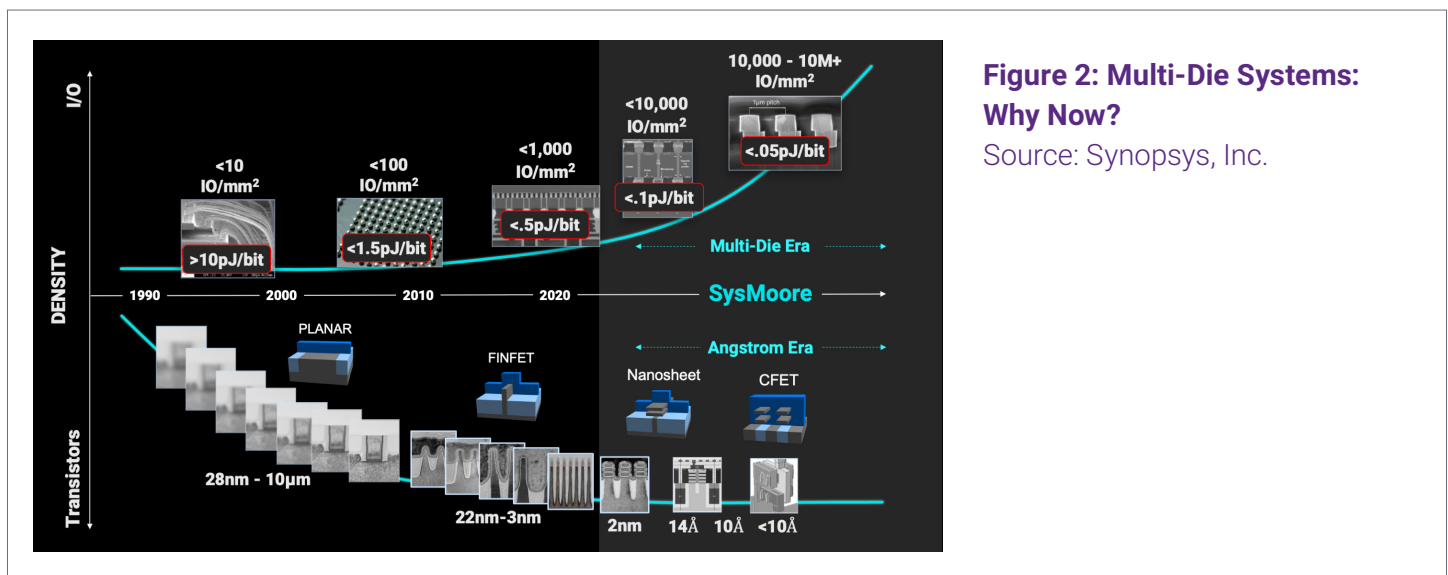


Figure 2: Multi-Die Systems: Why Now?

Source: Synopsys, Inc.

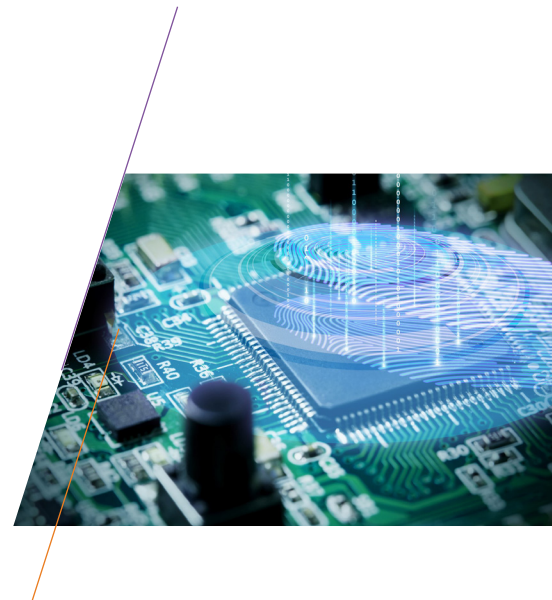
As angstrom-sized transistors intersect with multi-die Si-substrates, we see Classic Moore pass the baton to SysMoore and we are off to the races! Today, Synopsys tracks more than 100 multi-die designs. Be it through HW/SW digital twins, multi-die connectivity IP, or AI-driven chip design, we collaborate closely with the leading SysMoore companies of tomorrow.

It is important to recognize that **'systemic complexity'** is truly complex! For example, a system can be a car, a medical robot, or a Wall Street trading application. Each of these systems being defined by software, which, in turn, runs on hardware. The complexities of hardware then require awareness of the interdependency of speed and computation per watt, thermal and structural stress (just to name a few) – and, lest we forget, these Smart systems must also be Secure and Safe!

We often say, "success is the sum of our efforts..." But these ingredients are not additive; they are multiplicative. A single zero, and everybody gets zero! Be it the technical interaction of subsystems or the collaboration between companies, teams, or individuals — systemic complexity requires joint success. **'Smart Everything'** has found its teamwork enabler — **'SysMoore!'**

There is an enormous challenge and great beauty in this outlook. And just like Frank Lloyd Wright famously expanded design beyond the building into its surroundings, our joint endeavors will profoundly impact mankind in the coming decades.

I thank Gordon Moore for being 'the' coach, motivating us to "build the impossible!"



THE ECOSYSTEM VIEW

What follows are contributions from industry leaders – **how they are enabling and using multi-die systems.**

The perspectives offered here provide insight into the multi-die ecosystem, what has been achieved, what problems must still be addressed and what lies ahead. Contributing to this chapter are:

Ansys: Get Ready for the Three Big Challenges Facing Multi-Die Design

Arm: Unlocking Compute Performance with Advanced Technology

Bosch: Our Vision: Creation of an OPEN Ecosystem for Automotive SoCs based on Chiplets from Numerous Vendors

Google: The AI Revolution and Co-Design with Chiplets

Intel: The Future of Multi-Die Systems Lies in Silicon

Samsung: Heterogeneous Integration Platform for Next Generation Computing “Road to Beyond Moore”



Get Ready for the Three Big Challenges Facing Multi-Die Design

As traditional Moore's Law scaling approaches its physical limits, the quest for higher electronic system densities is transitioning to multi-die systems via 2.5D and 3D packaging technologies. The potential for more capable systems with higher yields is already impacting suppliers of high-performance computing (HPC) processors, graphics, and artificial intelligence/machine learning (AI/ML) enablement at the edge of the cloud. Multi-die technology represents an inflection point in electronic design. It is defining what it takes to build capable EDA flows.

Successful adoption of multi-die heterogeneous integration hinges on overcoming three challenges:

- Multiscale:** Advanced multi-die systems condense three design scales into one design challenge that crosses six orders of magnitude, from nanometer IC design, through millimeter package design, to centimeter 3D-IC systems. These solutions are divided into three tool suites (IC, systems, and packaging) that need to be integrated into [a single solution](#).
- Multiphysics:** Another immediate need is for a broader array of multiphysics analyses. Formerly second- or third-order effects — like [thermal management](#), [electromagnetic coupling](#), or [mechanical stress/warpage reliability](#) — become *the* primary limiting factors for multi-die design success. This introduces unfamiliar physics to many designers who will need automated analysis and signoff solutions to guide them.
- Multi-organizational:** The expertise to tackle multi-die design is often scattered across different teams in a company. Success in multi-die design requires much closer organizational coordination throughout the design process.



“Our partnership with Synopsys is making bespoke silicon possible, providing a unique differentiator for forward looking systems companies.”



Ajei Gopal

President and Chief Executive Officer, Ansys

Collaboration is the way forward

Beyond organizational coordination, a successful approach to multi-die design requires an integrated design flow. Best-in-class design and signoff solutions based on industry-leading products must be well integrated. Open, extendable platforms are also an important ingredient.

[Ansys](#) and [Synopsys](#) have collaborated to address these challenges with products like [Synopsys PrimeTime](#), [Fusion Compiler](#), [3DIC Compiler](#), and [Ansys RedHawk-SC](#). We are also promoting open environments based on standards and popular languages like [Python](#) that are a win-win for electronic designers and the EDA industry.

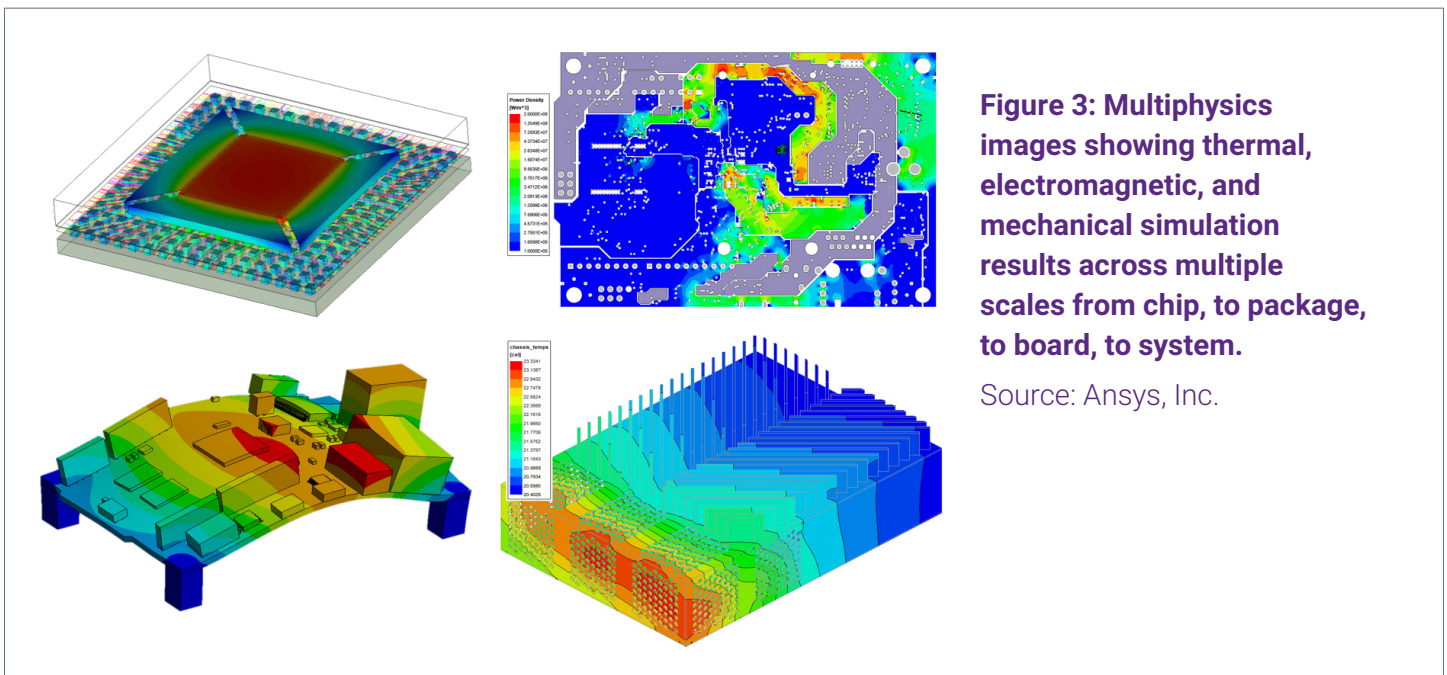


Figure 3: Multiphysics images showing thermal, electromagnetic, and mechanical simulation results across multiple scales from chip, to package, to board, to system.

Source: Ansys, Inc.

Unlocking Compute Performance with Advanced Technology

Unlocking the potential

The most advanced silicon processes provide fast, dense, highly power efficient digital logic. The combination of process with advances in the Arm architecture have driven up compute performance. This comes with a rise in the required memory bandwidth and has resulted in increasing complex cache hierarchies with increased on-die SRAM capacity. While logic has continued scaling, in recent years the SRAM density scaling has slowed. This has increased the cost of on-die SRAM, when compared to logic.

Advanced 2.5D and 3D chip-to-chip interconnect fills the 'pitch gap' between the PCB and on-die interconnect. To take advantage of this, Arm is developing architectures for compute subsystems to facilitate partitioning into chiplets, allowing systems to scale seamlessly across multiple dies. This allows high performance compute systems, such as cloud servers, to grow beyond the reticle limit, as well as use the process nodes best suited for each part of the system.

Looking to the future

As 2.5D and 3D advanced packaging becomes deployed more widely into a broader range of products, we enter a feedback loop. High volume increases yield and reduces cost, which enables new system partitions to address additional use cases. Interesting opportunities emerge to utilize the latest process nodes for advanced compute, while continuing to increase SRAM capacity in a cost-efficient way.

In the future, we believe systems composed of co-packaged chiplets will become widespread across the industry. Companies will be able to amortize their hardware and software engineering investment by reusing chiplets for multiple products. Complex systems will be cleanly partitioned, reducing risk, cost, and time to market.

arm

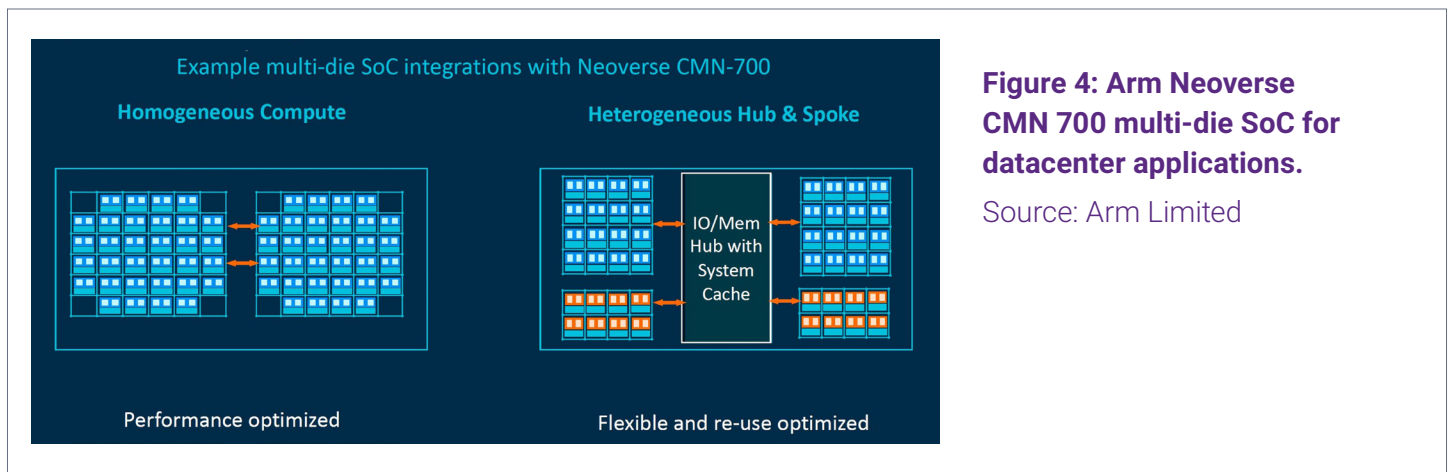
“Re-use of effort is at the core of the foundry and silicon-IP business models. This remains the key enabler which allows exciting new products to be put into the hands of consumers in a cost-efficient way.”



Gary Campbell

Executive Vice President,
Central Engineering, Arm

Re-use of effort is at the core of the foundry and silicon-IP business models. This remains the key enabler which allows exciting new products to be put into the hands of consumers in a cost-efficient way. Standardization is crucial to enable a truly interoperable chiplet ecosystem. Besides process and die-to-die interconnect technologies, suitable system architectures and IPs are required to provide composability through to the higher-level software interfaces. Arm looks forward to working with our industry partners to enable this future.



Our Vision: Creation of an OPEN Ecosystem for Automotive SoCs based on Chiplets from Numerous Vendors



Future vehicle computers require enhanced capabilities

These systems present high computation demands for central data processing with a wide range of functional integration. Examples include central software-driven platforms with service-oriented architectures, multiple operation systems, and a variety of safety, timing, and security demands.

There is a need for rapid update and innovation cycles with generation intervals of about two years. We see scalability demands across different models and with individual feature sets.

High-performance SoCs (especially for ADAS/AD and Infotainment) present challenges and opportunities

The optimization potential (performance, power, etc.) by technology carries over from consumer electronics or HPC designs at OEMs. However, there is insufficient scalability of SoCs across all vehicle classes and functions (e.g., from NCAP to SAE L4). The lack of resilient supply chains contributes to the problem.

“The time has come to evolve our ecosystem to a new level of multi-die sourcing and integration.”



Dr. Oliver Wolst

Senior Vice President Integrated Circuits, Bosch

“A vibrant chiplet ecosystem will unlock new innovation opportunities.”



Michael Schaffert

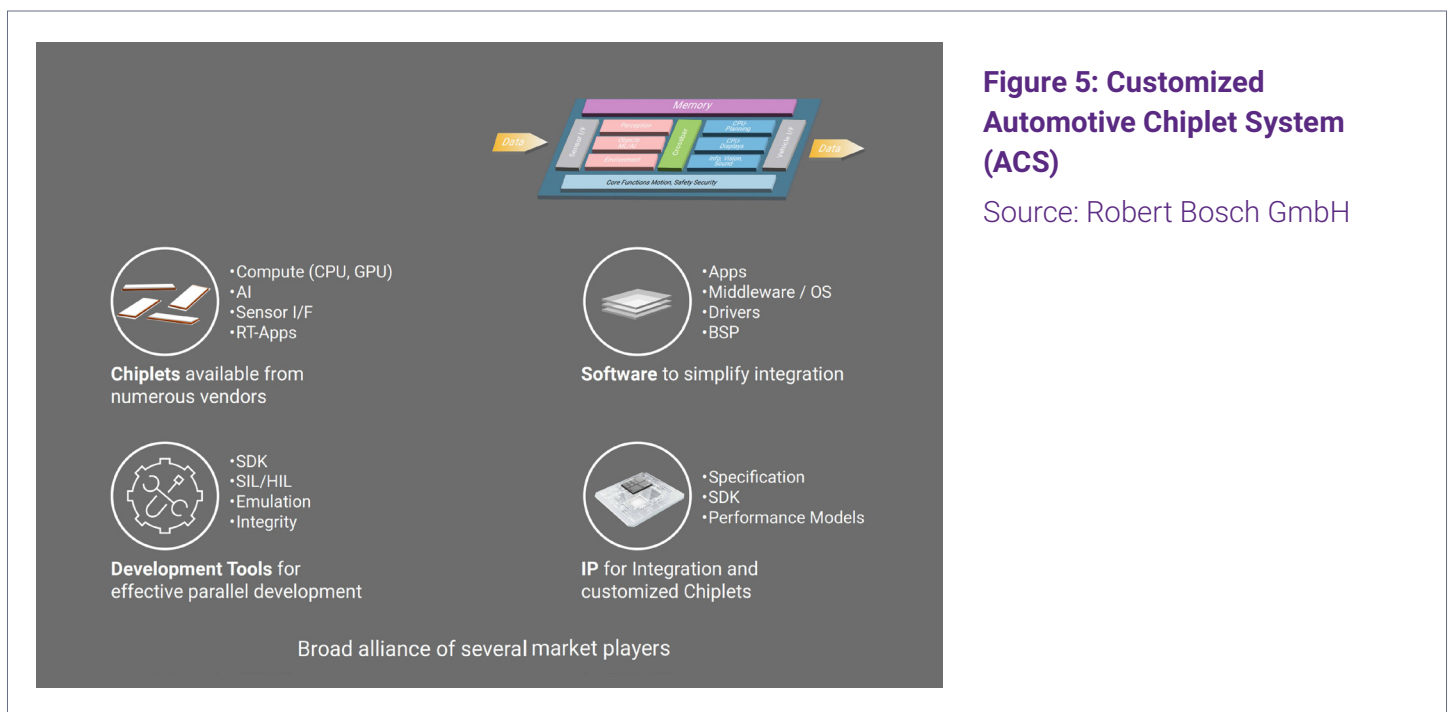
Senior Vice President E/E-Architecture, Bosch

To overcome these obstacles, a requirements-driven open ecosystem is needed

Automotive SoCs based on chiplets from numerous vendors provides the required level of flexibility and sophistication. A customized automotive chiplet system (ACS) can be based on design approaches proven in non-automotive, high-performance SoC design.

This will allow the break-up of a monolithic system into separate integrated circuits on multiple dies, integrated by advanced packaging technologies to comprise a high-performance compute unit.

What is needed is a market environment where system OEMs can reduce lead time to configure specific individual automotive chiplet systems, based on a chiplet offerings and related software and tooling from various suppliers.



Key characteristics of this OPEN EcoSystem:

- **Interfaces, connections, and standards** are **clearly defined** within the ecosystem
- **Each value chain step** is supported with a **multitude of players** that produce similar chiplets
- This approach delivers the highest degree of modularization and co-creation to enable **best, scalable products**

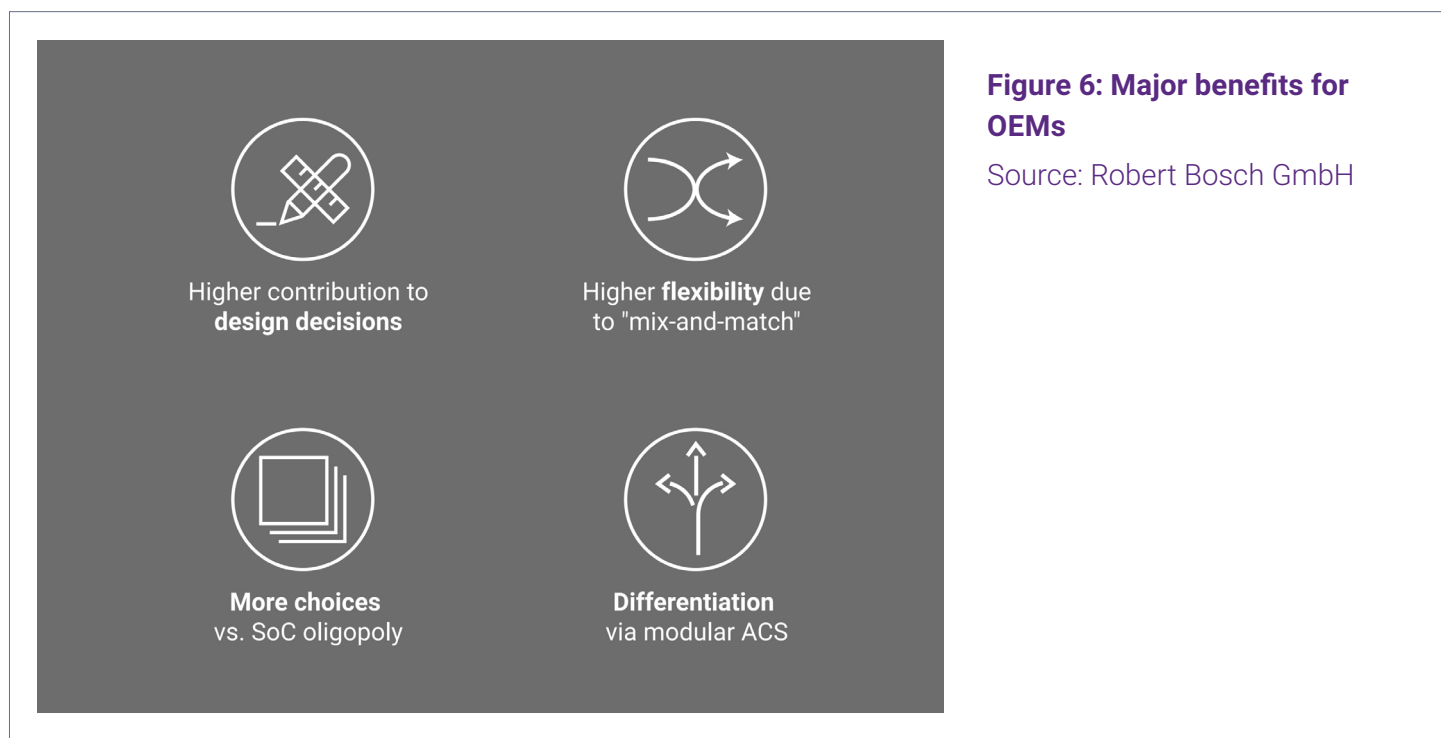


Figure 6: Major benefits for OEMs

Source: Robert Bosch GmbH

The AI Revolution and Co-Design with Chiplets



The AI revolution: The challenges ahead

The AI revolution is just getting started. Beyond large language models and generative AI, there is a lot of new innovation ahead in AI and ML. This accelerated pace of innovation on exponential volumes of data means a correspondingly profound increase in compute requirements.

But supply is not keeping up with this demand. Moore's law, which underpinned our computing innovations is slowing down. Chip geometries can no longer shrink at the rate we assumed they would. We are seeing generation-to-generation power and performance improvements slowing down drastically.

Put together, we need much more compute power than ever before, and traditional technology approaches do not support this growth. We have to evolve faster! *We need to revolutionize how we develop chips.*

The AI revolution: The opportunities ahead

It is time for a new framework to deliver advanced computing, to rewrite the rules of hardware innovation, *creating harmony between hardware and software.*

System-level optimization or co-design where we look at the whole stack – from the application level all the way down to the chip level – can achieve dramatic benefits. Our [Tensor Processing Units](#) (TPUs) and [Video Coding Units](#) (VCUs) have both adopted this approach to [sustainably](#) meet the growing demand for machine learning and video distribution services at Google.

We must look beyond traditional logic design and embrace modularity to take advantage of chiplets and packaging solutions. Chiplets allow us to do co-design in a multi-die system context, allowing cost advantages but also mix-and-match integration across heterogeneous IP blocks.

“The industry is at an exciting inflection point. Between AI and chiplets, we have the opportunity to create end-to-end entirely new, magical experiences that users have never seen – or even knew they needed – before.”



Partha Ranganathan

Google Fellow & Vice President Engineering, Google

There are a lot more pieces of the puzzle that will need to come together – across cooling, testing, standards, etc. – but one thing is sure: there is going to be a lot of innovation in the next few years ahead. *We are just getting started!*



Figure 7: A TPU v4 Pod contains 4,096 TPU v4 chips and delivers more than 1 exaflop / second of computing power. This TPU v4 Pod is in a datacenter that is operating at or near 90% carbon-free energy.

Source: Google LLC

The Future of Multi-Die Systems Lies in Silicon

Enabling advanced products with multi-die

In the pursuit of the greater functional integration of Moore's Law, 3D-IC integrates the silicon content within a package. With more functionality integrating within a package, where the system essentially collapses into the package, the amount of silicon exceeds that which can be built within lithography reticle limits.

The functionality must be split across multiple silicon components, with advanced packaging techniques providing low latency, low power, high bandwidth interconnections between the multiple chiplets.

System-Technology-Co-Optimization (STCO), the next major evolution of innovation in Moore's Law, starts tops down with application workloads and optimizes performance for those workloads with semiconductor technology vectors, multi-die chiplets, and advanced packaging interconnects.

STCO framework provides the optimized heterogeneous integration of each chiplet's design and silicon process features, cost, functionality, IP block availability, and with advanced packaging delivers optimized System-in-a-Package solutions.



"Multi-die technology with advanced packaging enables system boards to collapse into a package."



Dr. Ann B. Kelleher

Executive Vice President General Manager, Technology Development, Intel

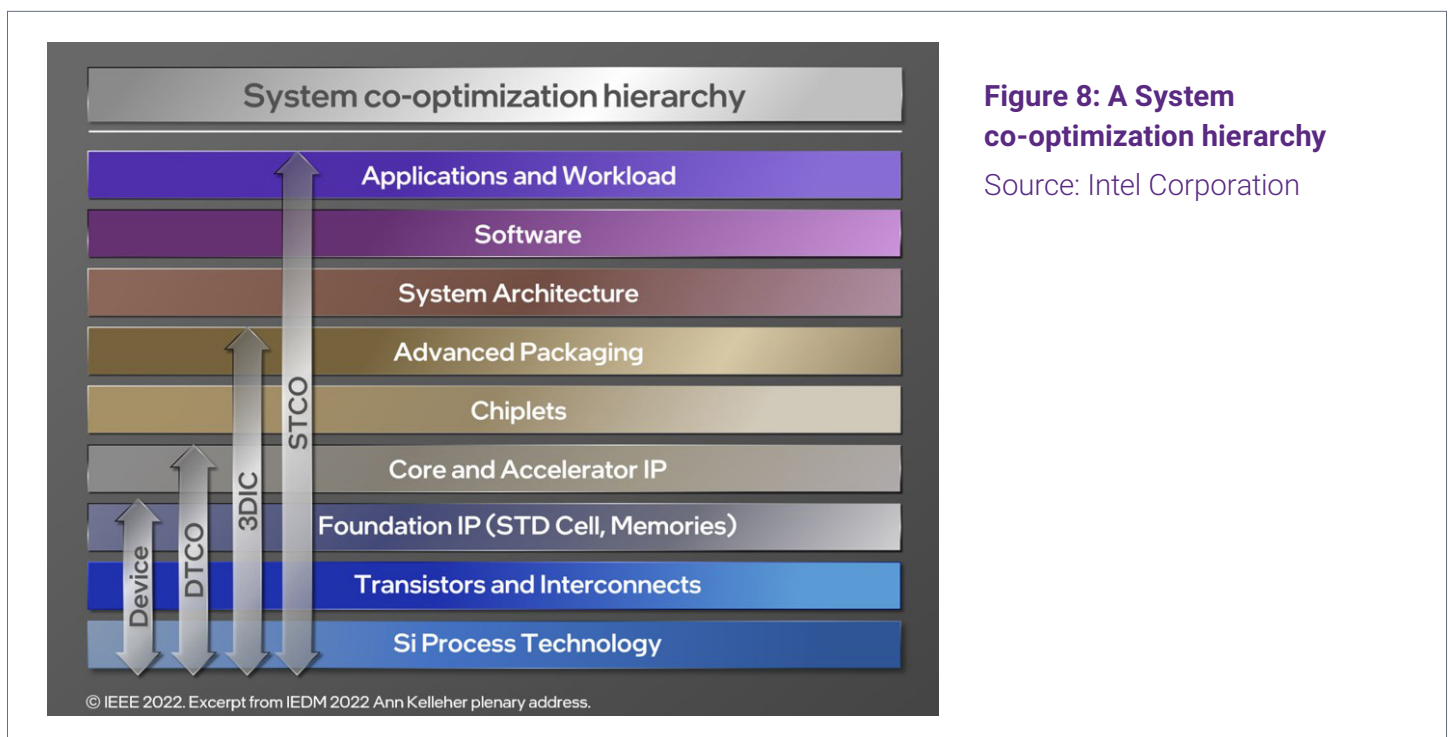


Figure 8: A System co-optimization hierarchy

Source: Intel Corporation

Enabling the ecosystem with advanced packaging

Advanced packaging plays a critical role in enabling multi-die products. Heterogeneous integration using advanced 2.5 and 3D packaging technologies, like EMIB and Foveros, offers an attractive path to architecting products by combining chiplets from various sources, designed on disparate silicon nodes.

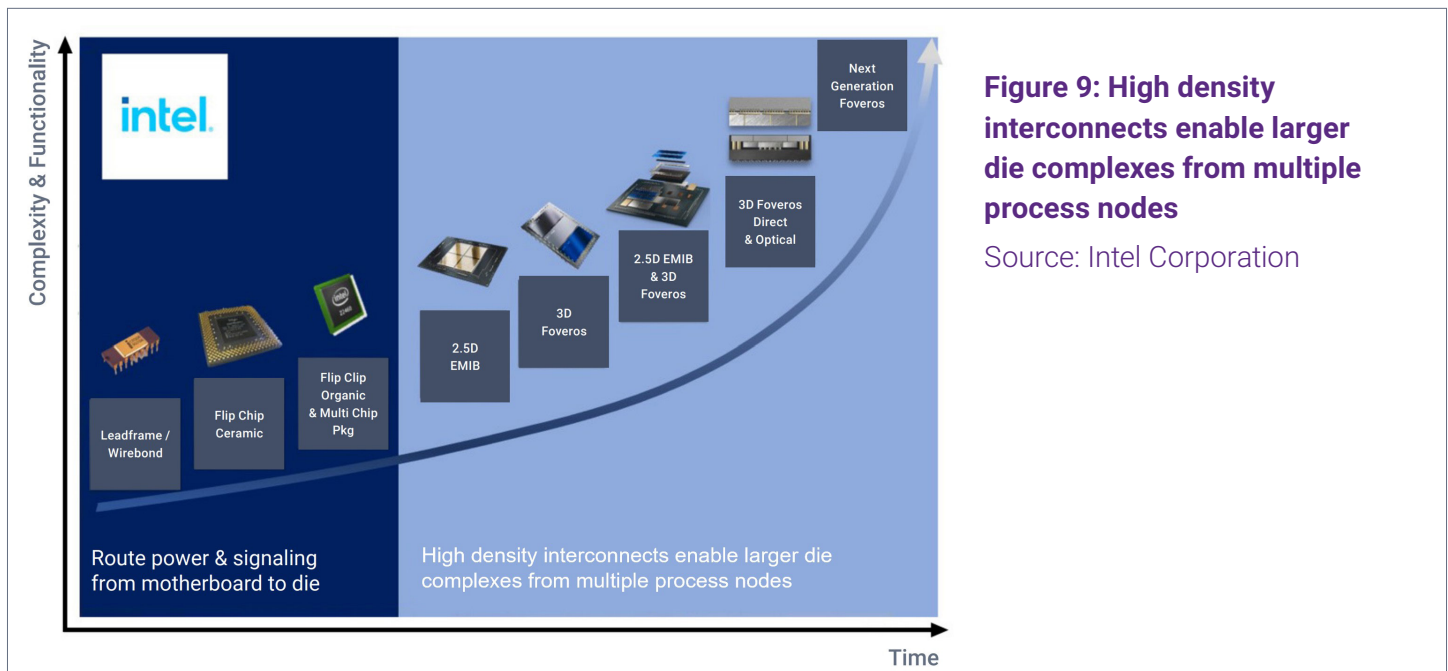


Figure 9: High density interconnects enable larger die complexes from multiple process nodes

Source: Intel Corporation

This mix and match capability unlocks the ability to optimize for unique functionality, performance, and cost while enabling reuse and modularity.

With this strategy there comes a key paradigm shift wherein packaging is now a key part of the overall co-optimization of the product system design. An important part of making an open chiplet ecosystem of multi-die integration more streamlined is standardization covering a multitude of elements, including die-to-die interfaces, design tools, mechanical specifications, and manufacturing equipment.

The Universal Chiplet Interconnect Express (UCIe) standard is one such standard and a crucial step in enabling the rich and robust industry ecosystem needed. On top of this, Electronic Design Automation (EDA) tools need to use standard file formats to enable seamless design among silicon, packaging, and system boards.

Intel Ponte Vecchio: Industry record for 3DIC integration

- >100 billion transistors
- 5 Nodes
- EMIB & Foveros
- 47 functional tiles

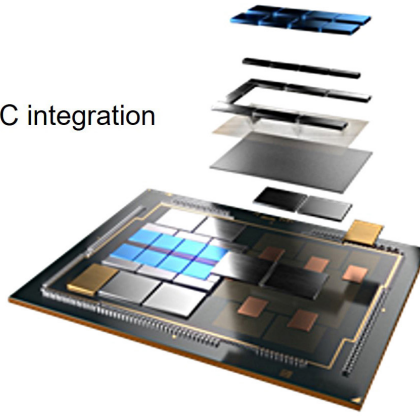


Figure 10: Multi-die technology in action

Source: Intel Corporation

Heterogeneous Integration Platform for Next Generation Computing “Road to Beyond Moore”

Breakthroughs in AI, 5G, autonomous vehicles and Metaverse tech promise to reshape the way we live – but delivering the function and performance needed to power those advancements on a single chip is becoming more complex, and less cost-effective.

Advances in heterogeneous chip packages are needed to empower today’s device manufacturers to pursue tomorrow’s breakthroughs. Both 2.xD and 3D variations will be needed to keep innovation vibrant.

Below are examples of how Samsung combines chips, process nodes, and cutting-edge tech to open new possibilities.

I-Cube 2.xD Package

2.xD packages deploy parallel horizontal chip placement to combat heat build-up and expand on performance. I-Cube Platform enables larger interposer, more HBMs and multi-die for AI/Data Center applications.

The I-CubeS based on Si-interposer brings impressive bandwidth and stunning performance capabilities to the table with emphatic warpage control, even with large interposers. And the I-CubeE has Si embedded structure which covers advantages of both Si-bridge by fine patterning and RDL interposer with TSV-less structure.



SAMSUNG

“Advanced Heterogeneous Integration opens the door to new levels of innovation for our customers.

Combining the power and diversity of today’s chips in a unified system brings new products within reach.”



Moonsoo Kang, Ph.D

Executive Vice President,
Advanced Package (AVP) Business,
Samsung Electronics

Figure 11: I-Cube 2.xD Package

Source: Samsung Electronics Co., Ltd.

X-Cube 3D IC

3D IC packages save massive amounts of on-chip real estate by stacking components vertically, reducing surface area and bumping performance by shortening the space between chips. By dramatically reducing the risks from big die construction, they keep costs low while retaining high bandwidth and low power performance.

X-Cube is a full 3D solution, which allows the vertical stacking of chips. X-Cube comes in two different forms: Two vertically stacked dies are connected either with micro bumps, or by bump-less hybrid Cu-Cu bonding (HCB). The HCB have a lot of advantages from the view-point of layout flexibility compared with the conventional chip stacking technologies.

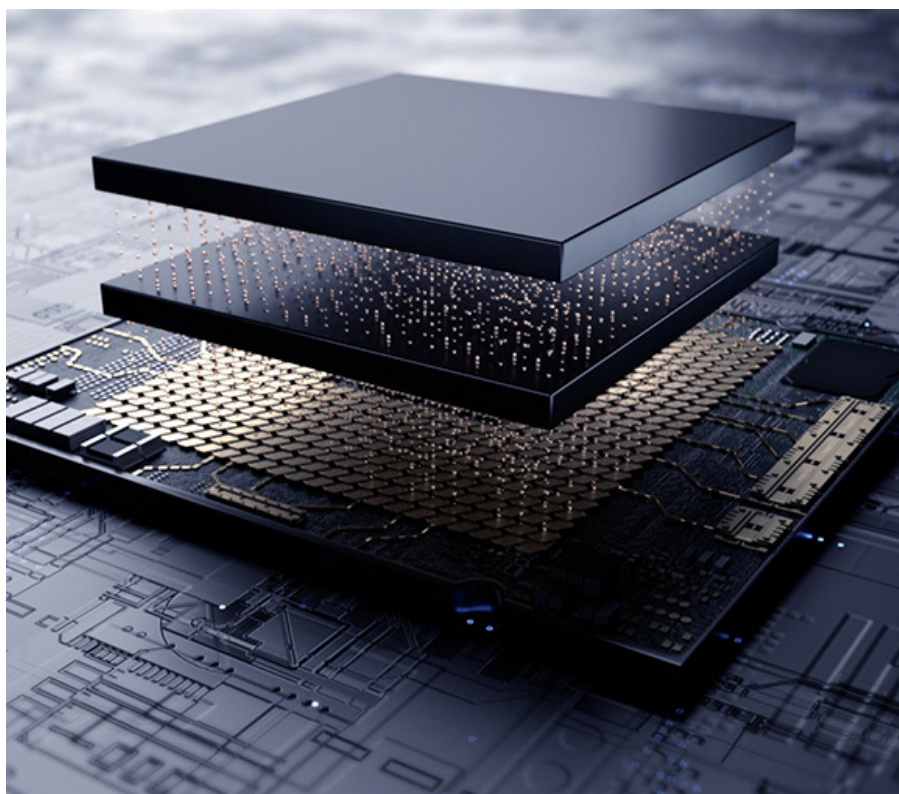


Figure 12: X-Cube 3D IC

Source: Samsung Electronics Co., Ltd.

Advanced Package Solution Service

Samsung launched a new advanced package (AVP) business unit for the increasing importance of Advanced Packaging. Build your way with end-to-end packaging solutions. Your products are unique. So are the chips that power them. Samsung AVP will provide flexible services to customers leveraging Samsung semiconductor's synergy platform. Samsung HI Ecosystem ensures deep collaboration between the Samsung AVP, ecosystem partners, and customers to deliver competitive and robust Advanced Package.

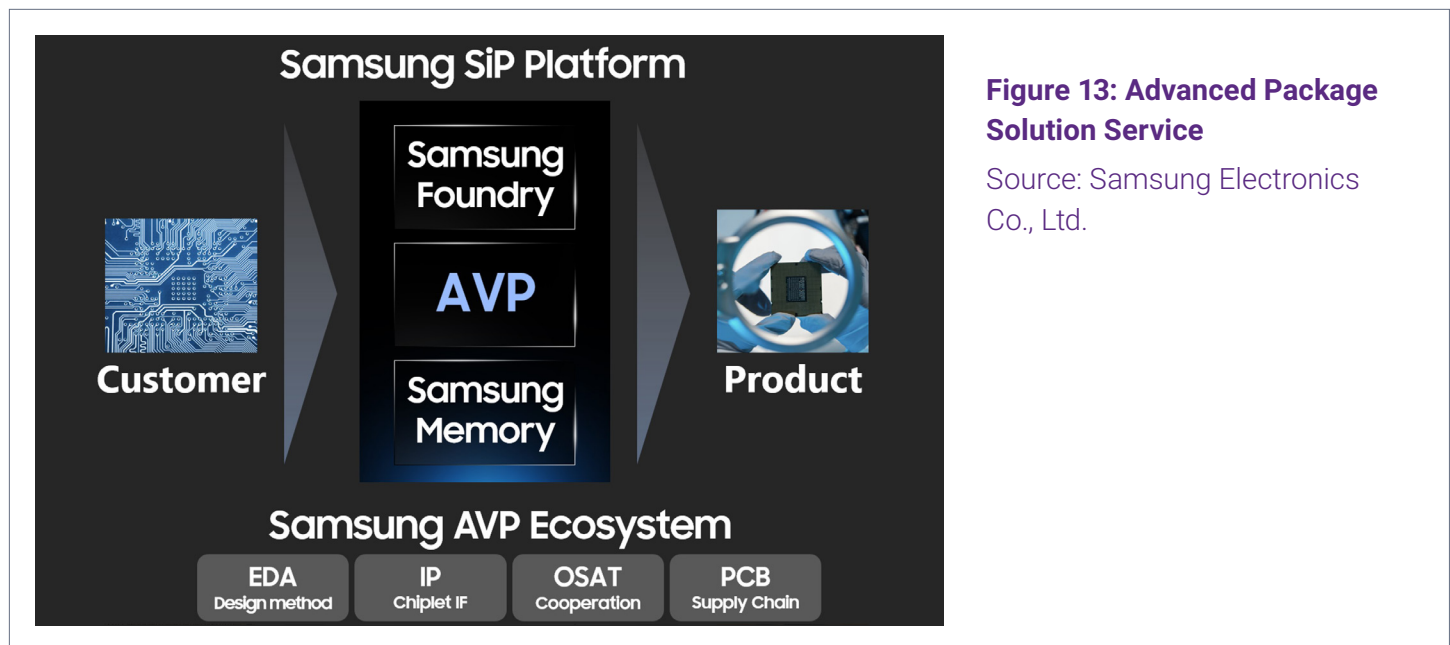


Figure 13: Advanced Package Solution Service

Source: Samsung Electronics Co., Ltd.

Samsung brings the benefits of multi-die integration to the mainstream — one unified system that is deeply efficient, highly adaptable, and simple to implement.

THE SYNOPSIS VIEW

This chapter summarizes views from Synopsys regarding multi-die systems – its growth, its challenges, and strategies to meet those challenges and bring the approach to mainstream access.

The information presented here is inspired by a roundtable discussion among Synopsys experts. There is a link to view the full video recording of that discussion at the end of the chapter. Synopsys staff participating in this discussion are:

Participating in that discussion were:

Rob Aitken, Distinguished architect and moderator of the discussion. Previous companies include Arm, Agilent, and Hewlett Packard. PhD in Electrical Engineering from McGill University.

Rita Horner, System solutions director. Deep expertise in design of advanced semiconductors and high-performance computing. Previous companies include Avago, Agilent, Hewlett Packard and Intel. BS and MS in Electrical Engineering from University of Tennessee, Knoxville.

Shekhar Kapoor, Senior product line director. Deep expertise in design tool and solution development. Previous companies include IBM Business Consulting, IBM Microelectronics, and LSI Logic. MS in Computer Engineering, Virginia Tech and MBA, University of California, Berkeley Haas School of Business.

Manmeet Walia, Product management director. Deep expertise in IP application and development. Previous companies include Toshiba, Exar and AMCC. BS and MS in Electrical Engineering, The University of Toledo and MBA, San Diego State University.

There is a link to view the full video recording of that discussion at the end of this chapter.



Why multi-die systems, why now?

At the very core of the movement to multi-die systems is the insatiable thirst for faster, better, and smarter. The drive to cram more and more functionality, and with that more user experiences into products and services. For many years, Moore's law-driven scalability met these needs.

However, device scaling is slowing and the benefits of moving to newer nodes are diminishing while costs are increasing — trends that will continue as we get into the Angstrom era. Yet the drive for compute, further fueled by ubiquitous AI is creating immense demand for highly complex and increasingly heterogeneous systems to address functionality and user experience needs.

The situation presents a perfect storm. If the chips can't scale as an answer to the growing compute-density and functionality demands, and the market demands these complex systems — we need a different answer. And that answer is multi-die systems.

How real is the multi-die system trend?

Simply put, it's very real and it's happening now. Synopsys works with many advanced system OEMs to develop next-generation semiconductor designs. We've already worked with quite a few customers to integrate multiple dies into a single package.

The economic benefits of a multi-die system approach include re-use of proven chip technology to create multiple SKUs in a product family. Large designs that approach the reticle limit, or maximum die size suffer from low yield, resulting in high silicon cost. Decomposing a large design into smaller chips results in much better yield and associated silicon cost.

From a physics perspective, ubiquitous sensing, analog processing and many types of communication don't benefit from advanced scaling. A system composed of optimized blocks, built with the optimal process technology presents a better alternative.

In November 2022, Synopsys held its yearly Global User Survey. 6,025 people responded to the survey which touched on many design and technology trends. The companies responding had a worldwide footprint and the respondents came from a broad range of job categories and disciplines.

A question regarding multi-die system usage revealed a strong adoption trend. The question asked respondents about plans to use 3D-IC technology, including thru-silicon vias (TSVs). Over 50% of respondents were either using or planning to use this technology.



How does the multi-die system approach impact the design flow?

All of the challenges faced in monolithic 2D chip design still must be addressed for multi-die systems. But the scale is much larger. The potential interactions between parts of the system are also greater. There are complex thermal and power management challenges within the package, architectural partitioning, and partitioning for the massive software stacks that interact with the hardware for example.

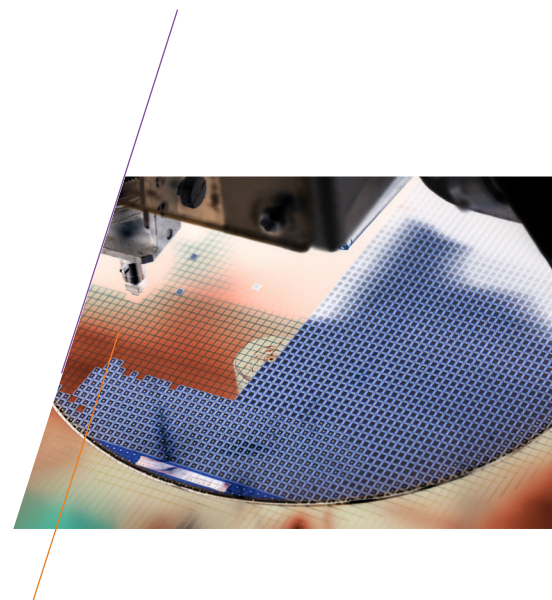
The multi-die system journey begins with partitioning between hardware and software. Each of the dies in a multi-die system could have its own software stack. And verifying this software in the context of the hardware it's going to run on is important. Synopsys has very successful solutions available for monolithic 2D chip design, and we've expanded those to enable the more complex verification problem presented by multi-die systems.

We have solutions like Platform Architect for early functional architectural exploration, and Virtualizer with the largest System C IP library to enable efficient virtual prototype assembly. And the HAPS prototype system, which delivers high-speed I/O verification as well as mixed voltage support. We offer the ZeBu and ZeBu Hybrid emulation platforms with very high scalability, which can handle the many use cases encountered in a complex multi-die system.

There are also unique power and thermal challenges. These become first-order effects and must be analyzed very early. To address this need we've partnered with Ansys to bring their best-in-class solutions for signal, power and thermal integrity into the design flow, alongside Synopsys' golden signoff solutions, PrimeTime and StarRC. This is all delivered with the 3DIC Compiler solution that provides a unified platform to integrate tens to hundreds of heterogeneous dies in an optimized system for performance, power, and thermal effects

Beyond design tools and methodology, IP is a critical enabler for multi-die systems. IP that fuels chiplet design and IP that facilitates communication between the dies in a multi-die system. Synopsys has the broadest IP portfolio in the industry with leading offerings across many titles, including a comprehensive die-to-die IP solution.

As we approach the end of the design process, system testability and reliability become important. The challenge here is not just taking all known good die and putting them together in a single package, it's about ensuring the health of the system all the way through its lifecycle, including in-field operation.



Synopsys has many solutions here like the extended TestMAX, as well as a portfolio to support silicon lifecycle management with tools, in-chip monitor IP and analytics to help the system through its journey in the field with reliability and security.

So, the [entire multi-die system journey is covered](#) from early architecture, to physical design and verification to deployment in the field.

Where do chiplets fit?

The term *chiplet* has many meanings. In general, a chiplet represents a bare-die version of a chip design that can be integrated with other components using high-density integration methods to form a complete system in a package. Chiplets can be used to implement small functions such as sensors all the way to large processor arrays that are as big as large monolithic designs.

For example, a popular use case is I/O disaggregation where compute engines are in one die and I/O are in a separate die. Enabling effective use of chiplets requires focus in two areas.

One is standardization of use cases for chiplets, such as the work being done by UCIe. This work addresses aspects such as electrical parameters, compliance with other standards, interoperability, and form factor.

The other is the supporting methodology, such as top-level partitioning, software development, testability, and silicon lifecycle management.


Both areas are important for the development of an industry-level chiplet ecosystem.

At Synopsys, we have the IP, the IP subsystems, the tools, methodologies and flows to help enable a chiplet ecosystem. We are also working with organizations such as the ODSA, part of OCP and the UCIe Consortium, along with all their partners and members to address the technical and the business challenges so multi-die systems can have broader adoption across the market.

Synopsys is also [introducing AI](#) into the multi-die system design flow to deliver step-function improvements in design efficiency and quality of results.

Synopsys experts discuss multi-die system design

[Learn more](#) about the full roundtable discussion that inspired the comments in this chapter.



The video thumbnail shows four people in a roundtable discussion. The Synopsys logo is in the top left. Text on the thumbnail includes 'THOUGHT LEADERSHIP', 'Synopsys Experts Discuss Multi-Die System Design', and a 'Watch Now >' button.

Synopsys experts discuss multi-die system design

[Watch video](#)

CHAPTER 4

A LOOK TO THE FUTURE

You've just read the thoughts of a broad base of multi-die system experts from across the technology sector. These are some of the industry leaders most involved in guiding its direction. For further insight, you can also read the [MIT Technology Review Insights report](#) published recently, 'Multi-die systems define the future of semiconductors' to hear from partners such as TSMC, Mercedes-Benz, Google, AMD, and industry analyst Patrick Moorhead. Echoing some of the collective thoughts, I'd like to offer my perspective informed by conversations with many key multi-die ecosystem participants.

First, I think everyone recognizes the need for disruptive ideas like the ones you've just read about as some areas of multi-die exploration, such as 3D systems of chips, are still in the R&D phase. It's rather like when in 2017 a team of Synopsys engineers proposed we create AI-based chip design technology. It was a huge stretch at the time, but fast-forward six years and the team has just rolled out a full AI-driven EDA suite covering digital design, analog, verification, test, and manufacturing – an industry first. It will be a key vehicle in delivering complex multi-die systems at scale.

For multi-die system, the list of "to dos" is long and it's not just about the technology. Our ecosystem partners all have their own approach, but the key challenges distill down to how to reduce the design effort required to build heterogeneous multi-die systems; less effort equals lower cost. To achieve this will require a collaborative multi-die ecosystem. This ecosystem will include many disciplines.



Sassine Ghazi

President and Chief Operating Officer, Synopsys

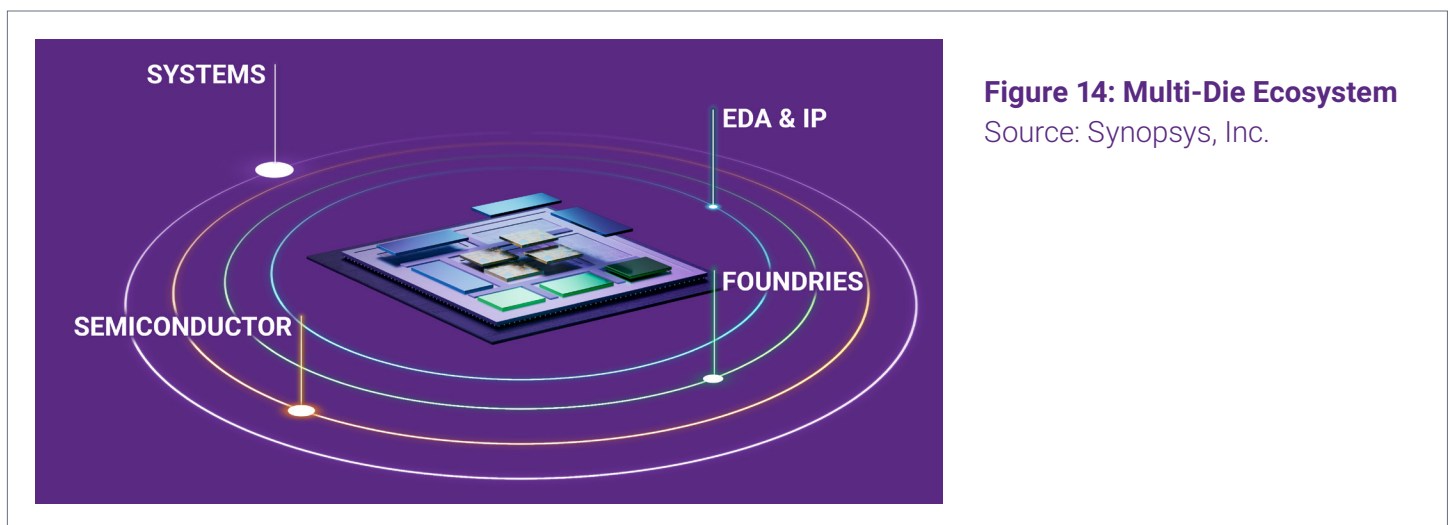


Figure 14: Multi-Die Ecosystem

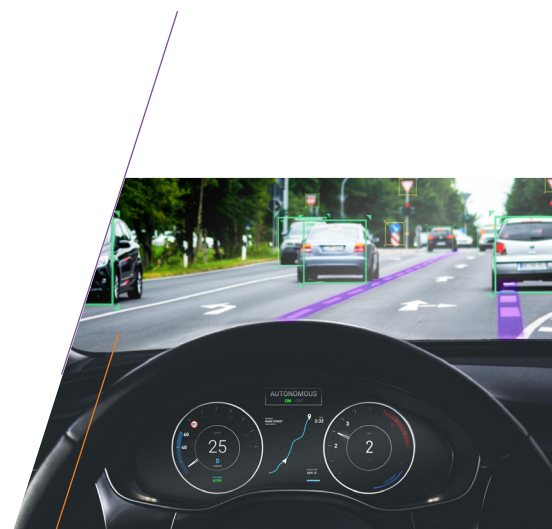
Source: Synopsys, Inc.

Expectations for the future of multi-die systems

My opinions on multi-die systems are based on internal engineering insight and the many hours I'm privileged to spend with senior leaders from the most advanced technology companies. That combined knowledge has given me the confidence to now predict the current trickle of high-end multi-die systems will become a flood spanning every applicable market before we reach the 2030s. I say this because of the rapid progress I see, not only in Synopsys' engineering labs but also the billions of dollars of secure investment going into multi-die systems from across public and private sources.

Specific examples include how we're now able to fuse architectural analysis and implementation as part of multi-die system flows. And recently, the addition of AI for a step-function increase in productivity and quality of results is inching us closer to scale. Even now, our customers and partners are designing products that appeared completely out of reach just a few years ago.

Multi-die systems are a subject that Synopsys and the technology sector at large care deeply about, and you'll hear much more from us as new capabilities evolve over the next few years. For Synopsys' part, we're honored that more than 95% of advanced chips today are built using Synopsys technology. We're tracking over 100 multi-die system designs today, with an uptick of 20% over the last six months and that tells me that this is a design direction which is maturing very fast indeed.



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